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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,750	09/25/2003	Chad A. Cobbley	MICS:0078--1 (FLE/MAN) (0	1056

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EXAMINER	
BLUM, DAVID S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,750	COBBLEY ET AL.	
	Examiner	Art Unit	
	David S Blum	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2004*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35,37-39,45,47-49,63 and 65-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *35,37-39,45,47-49,63 and 65-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This action is in response to the amendment filed 09/07/04.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 35, 37-39, 45, 47-49, 63, and 65-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pai (US006503776B2) in view of Huang (US006753206B2).

Pai teaches the device of claims 35, 37-39, 45, 47-49, 63, and 65-67 as except for each die in the stack being functional (in an electrical sense) and the stack being a shingle stack (defined in the instant specification where the die centers are not aligned).

Claim 35. An integrated circuit comprising:

a stack comprising at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the semiconductor die being coupled together by a first adhesive, the first adhesive **(166)** being curable at a first temperature; and

a substrate coupled **(substrate 120 coupled to stack through chip 110 and adhesive 162)** to one of the at least two semiconductor die by a second adhesive **(112)**, the second adhesive being curable at a second temperature lower than the first temperature; **(it is noted that Pai teaches this (column 3 lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight.**
Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack of at least two semiconductor die is functional **(Pai teaches a dummy die, the dummy die serving a function, thus being functional. The instant specification teaches that each die is tested to be functional, and in light of the specification, the examiner believes that Pai reads on this limitation of being functional. Huang forms a stack similar to that of Pai, but teaches a stack where all die are "electrically" functional. It would be obvious to one skilled in the art to modify Pai by using an electrically functional die in the stack as taught by Huang.**

Claim 37. The integrated circuit, as set forth in claim 35, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die **(See figure 10)**.

Claim 38. Claim 35. An integrated circuit comprising:

a stack comprising at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the semiconductor die being coupled together by a first adhesive, the first adhesive **(166)** being curable at a first temperature; and

a substrate coupled **(substrate 120 coupled to stack through chip 110 and adhesive 162)** to one of the at least two semiconductor die by a second adhesive **(112)**, the second adhesive being curable at a second temperature lower than the first temperature; **(It is noted that Pai teaches this (column 3 lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight.**
Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack **(Huang teaches a conventional stack (prior art) and a shingle stack (figures 2 and 5) with the advantage of being able to package chips of various sizes (column 2 lines 45-47)) Further, it is noted that the instant application teaches a "conventional** .

Claim 39. The integrated circuit, as set forth in claim 35, wherein at least one of the at least two semiconductor die comprises a memory die **(column 1 line 18)**.

Claim 45. An integrated circuit comprising a stack of at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the die being coupled to an adjacent die in the stack **(110)** by a respective layer of adhesive **(162)** prior to the stack being coupled to a packaging substrate. **(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)**

wherein each die in the stack of at least two semiconductor die is functional **(Pai teaches a dummy die, the dummy die serving a function, thus being functional. The instant specification teaches that each die is tested to be functional, and in light of the specification, the examiner believes that Pai reads on this limitation of being functional. Huang forms a stack similar to that of Pai, but teaches a stack where all die are "electrically" functional. It would be obvious to one skilled in the**

art to modify Pai by using an electrically functional die in the stack as taught by Huang.

Claim 47. The integrated circuit, as set forth in claim 45, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die (**See figure 10**).

Claim 48. An integrated circuit comprising a stack of at least two semiconductor die (**130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20**), each of the die being coupled to an adjacent die in the stack (**110**) by a respective layer of adhesive (**162**) prior to the stack being coupled to a packaging substrate; (**The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113**)

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack (**Huang teaches a conventional stack (prior art) and a shingle stack (figures 2 and 5) with the advantage of being able to package chips of various sizes (column 2 lines 45-47)**).

Claim 49. The integrated circuit, as set forth in claim 45, wherein at least one of the at least two semiconductor die comprises a memory die **(column 1 line 18)**.

Claim 63. An integrate circuit package comprising:

a substrate **(120)**; and

a die stack coupled to the substrate **(Figure 10)**, wherein the die stack comprises at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)** coupled together and wherein the dies stack is formed prior to being coupled to the substrate;

(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack of at least two semiconductor die is functional **(Pai teaches a dummy die, the dummy die serving a function, thus being functional. The instant specification teaches that each die is tested to be functional, and in light of the specification, the examiner believes that Pai reads on this limitation of being functional. Huang forms a stack similar to that of Pai, but teaches a stack**

where all die are "electrically" functional. It would be obvious to one skilled in the art to modify Pai by using an electrically functional die in the stack as taught by Huang.

Claim 65. The integrated circuit package, as set forth in claim 63, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die **(See figure 10)**.

Claim 66. Claim 63. An integrate circuit package comprising:

a substrate **(120)**; and

a die stack coupled to the substrate **(Figure 10)**, wherein the die stack comprises at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)** coupled together and wherein the dies stack is formed prior to being coupled to the substrate;

(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack **(Huang teaches a conventional stack (prior art) and a shingle stack (figures 2 and 5) with the advantage of being able to package chips of various sizes (column 2 lines 45-47))**.

Claim 67. The integrated circuit package, as set forth in claim 63, wherein at least one of the at least two semiconductor die comprises a memory die **(column 1 line 18)**.

It would be obvious to one skilled in the requisite art at the time of the invention would modify Pai by including an electrically functional die and a shingle stack as taught by Huang to be an improvement with chips of varied sizes **(Huang teaches a conventional stack (prior art) and a shingle stack (figures 2 and 5) with the advantage of being able to package chips of various sizes (column 2 lines 45-47))**.

3. Claims 68-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pai (US006503776B2) in view of Hakey (US006627477B1) or Moden (US006512303B2).

Pai teaches the device of claims 68-70 as except for explicitly teaching that each die in the stack may successively thinner than the previous one.

Claim 68. An integrated circuit comprising:

a stack comprising at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the semiconductor die being coupled together by a first adhesive, the first adhesive **(166)** being curable at a first temperature; and

a substrate coupled **(substrate 120 coupled to stack through chip 110 and adhesive 162)** to one of the at least two semiconductor die by a second adhesive **(112)**, the second adhesive being curable at a second temperature lower than the first temperature; **(it is noted that Pai teaches this (column 3 lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight.**
Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack of at least two die is successively thinner than the previous die (**Pai teaches combining chips of processor, memory and associated logic into a single package (column 1 lines 17-19). Although not teaching that these chips may have a different thickness from each other, one skilled in the requisite art would know this. Hakey does not stack the die, but also connects die of logic chips and memory chips and teaches that these die have different thicknesses (column 2 lines 34-40), thus confirming that one would know that the**

chips of Pai could be of a different thickness from each other. Further, Moden teaches stacking and coupling chips having a different thickness (figure 4), thus it is known to stack chips (as Pai's stack) having a different thickness. In a stack of two die of different thicknesses, it is inherent that one die be successively thinner than the previous die).

Claim 69. An integrated circuit comprising a stack of at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the die being coupled to an adjacent die in the stack **(110)** by a respective layer of adhesive **(162)** prior to the stack being coupled to a packaging substrate; **(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)**

wherein each die in the stack of at least two die is successively thinner than the previous die (**Pai teaches combining chips of processor, memory and associated logic into a single package (column 1 lines 17-19). Although not teaching that these chips may have a different thickness from each other, one skilled in the requisite art would know this. Hakey does not stack the die, but also connects die**

of logic chips and memory chips and teaches that these die have different thicknesses (column 2 lines 34-40), thus confirming that one would know that the chips of Pai could be of a different thickness from each other. Further, Moden teaches stacking and coupling chips having a different thickness (figure 4), thus it is known to stack chips (as Pai's stack) having a different thickness. In a stack of two die of different thicknesses, it is inherent that one die be successively thinner than the previous die).

Claim 70. An integrate circuit package comprising:

a substrate **(120)**; and

a die stack coupled to the substrate **(Figure 10)**, wherein the die stack comprises at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)** coupled together and wherein the dies stack is formed prior to being coupled to the substrate;

(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack is successively thinner than the previous die (**Pai teaches combining chips of processor, memory and associated logic into a single package (column 1 lines 17-19). Although not teaching that these chips may have a different thickness from each other, one skilled in the requisite art would know this. Hakey does not stack the die, but also connects die of logic chips and memory chips and teaches that these die have different thicknesses (column 2 lines 34-40), thus confirming that one would know that the chips of Pai could be of a different thickness from each other. Further, Moden teaches stacking and coupling chips having a different thickness (figure 4), thus it is known to stack chips (as Pai's stack) having a different thickness. In a stack of two die of different thicknesses, it is inherent that one die be successively thinner than the previous die).**

It would be obvious to one skilled in the requisite art at the time of the invention to modify Pai to include chips having a different thickness as suggested by Pai's description of the chips, Hakey teaching that the chips listed by Pai have different thicknesses, and by Moden teaching that it is known to stack chips of different thicknesses.

Response to Arguments

4. Applicant's arguments with respect to claims 35, 37-39, 45, 47-49, 63, and 65-67 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the added limitation that each die be functional, the dummy die of Pai serves a function, therefore is functional. The instant specification teaches that the chips are tested to be functional, but does not teach what functional is. The dummy chip of Pai reads on this. Huang has been added to show that one skilled in the requisite art would recognize that an electrically functional die could be used in lieu of the dummy die of Pai.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (757)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (703) 872-9306. The facsimile number for customer service is (703)-872-9317.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David S. Blum

November 29, 2004